# Modified Binary Multiplier Circuit Based on Vedic Mathematics

# Abstract:

This paper presents a modified binary multiplier using Vedic mathematics. The paper proposes a modification in the previously published Vedic multiplier circuit. The suggested modified Vedic multiplication technique is more efficient in terms of delay and area. The proposed circuit is implemented in VeriLog. The Mentor Graphics ModelSim tool is used for HDL simulation, and the Xilinx ISE Design Suite 14.1 is used for circuit synthesis. The simulation is done for 4-bit, 8-bit, and 16-bit multiplication operations. In this paper, the simulation waveforms are shown only for 4-bit multiplication operation based on the modified Vedic multiplication technique. The proposed method can be extended for a larger bit size. The performance evaluation in terms of speed and device utilization is compared with the previously reported Vedic multiplier architectures. The proposed design exhibits a speed improvement compared to the multiplier architectures available in literature.

**Tools used:**

**Xilinx 13.2**